FPGA Upgrade Proposals for the Hall B Torus and Solenoid Control and Monitoring Systems

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August 28, 2019

The Low Voltage chassis (LV chassis) of Hall B's Torus and Solenoid control and monitoring systems use Terasic's DEO-Nano boards instrumented with Altera Cyclone IV FPGAs, which communicate with the Torus/Sol PLCs via RS-232 interfaces to the National Instruments (NI) serial modules in the Torus/Sol LV cRIO chassis and the LabVIEW EtherNet/IP real-time Ethernet protocol software. This note presents two methods for upgrading the current LV chassis, which would obviate the Torus/Sol LV cRIO chassis, and thereby reduce hardware and software complexity and increase system reliability.

Hall B's Torus and Solenoid control and monitoring systems' eight custom-built LV chassis [1], each equipped with Altera Cyclone IV FPGA on a Terasic DE0-Nano development board, power the instrumentation sensors and communicate via RS-232 with the NI serial modules in the Torus/Sol LV cRIO chassis, whose controllers interface with the Torus/Sol PLCs using LabVIEW EtherNet/IP [2] real-time Ethernet protocol, Fig. 1.

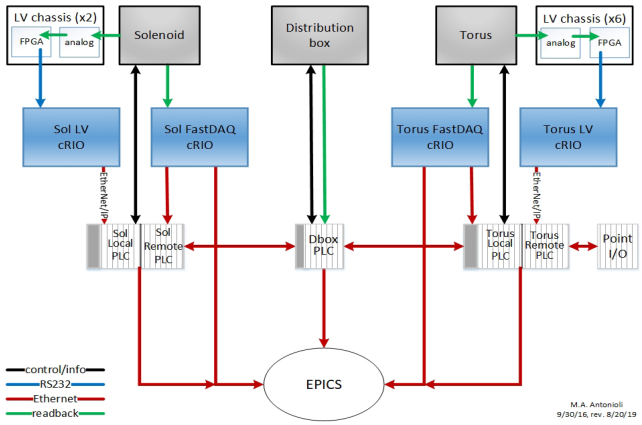

FIG. 1. Torus and Solenoid control and monitoring systems.

Recently, Terasic introduced the DE0-Nano-SoC Kit [3] equipped with the Altera Cyclone V System-on-Chip (SoC), Fig. 2. Upgrading the LV chassis with the DE0-Nano-SoC Kit would remove the need for the Torus/Sol LV cRIO chassis.

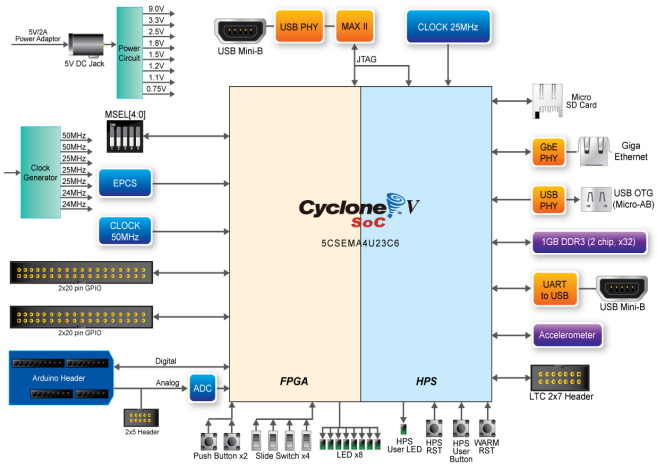

FIG. 2. DEO-Nano-SoC block diagram [3].

The first method of upgrading the LV chassis with the new DE0-Nano-SoC running Linux would be to develop software for *communication* between the FPGA and the HPS in the SoC, Fig. 2, and for *communication* between the SoC and PLCs, Fig. 3. This version of the upgrade would eliminate the Torus/Sol LV cRIO chassis and the EtherNet/IP real-time Ethernet protocol software.

The second method of upgrading the LV chassis would be to implement an NI sbRIO [4] with software developed by the Detector Support Group (DSG) [5–6]. This version of the upgrade would use LabVIEW EtherNet/IP real-time Ethernet protocol software, Fig. 3. In this version of the upgrade, in addition to eliminating the Torus/Sol LV cRIO chassis, it would unify and streamline the maintenance of Hall B's control and monitoring systems.

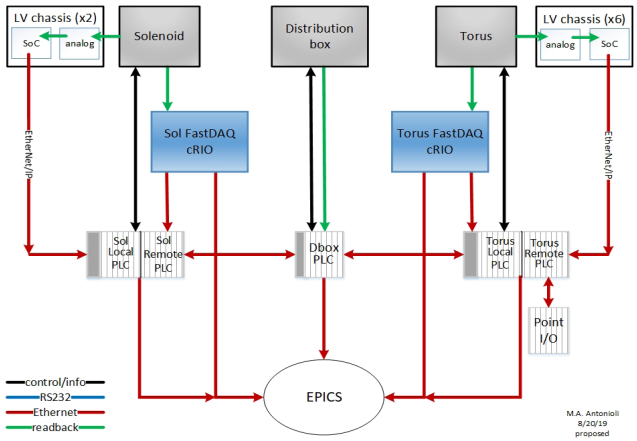

FIG. 3. Proposed Torus and Solenoid control and monitoring system. Version one of the upgrade uses special software developed for communication between the LV chassis and the PLCs. The EtherNet/IP real time protocol software indicated by the label on the red line between the LV chassis and the Torus/Sol PLCs will not be needed. Upgrade version two does use the EtherNet/IP real time protocol software. Both versions of the upgrade eliminate the Torus/Sol LV cRIO.

To conclude, DSG is proposing two ways of upgrading the LV chassis, each of which eliminates the Torus/Sol LV cRIO chassis, thereby reducing the system's hardware and software complexity and increasing system reliability.

[1] P K Ghoshal, et al. *Instrumentation and Control Selection for the 12GeV Hall B Magnets at Jefferson Lab,* Supercond. Sci. Technol. 31 (2018) 095007.
[2] National Instruments EtherNet/IP, http://sine.ni.com/nips/cds/view/p/lang/en/nid/209676.
[3] Terasic DE0-Nano-SoC Kit, https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=941.
[4] National Instruments (2017) *NI sbRIO-9627: User Manual* Retrieved from http://www.ni.com/pdf/manuals/375466b.pdf.
[5] P. Bonneau, et al. *Proposed Controller for the Readout of the Temperature and Humidity Digital Sensors Sensirion SHT85 Envisioned for the RICH Detector*, DSG Note 2019-27, 2019.
[6] P. Bonneau, et al. *Development of Data Acquisition to Read out Sensirion SHT85 Temperature and Humidity Sensors for the RICH Detector,* DSG Note 2019-31, 2019.